REMARKS

Applicants have amended claims 23, 31 and 73, and added new claims 78-81 to more fully claim the invention. Claim 78 depends from claim 73, and recites that the thermal conductivity of the stratum is about 1 W/m/K or less. Support for claim 78 appears in the specification as originally filed. See, for example, page 26, lines 24-27 of the specification.

Independent claim 79 recites a method of generating a temperature gradient that uses a stratum comprising materials selected from the group consisting of glass, silicon and plastic. Support for claim 79 appears in the specification as originally filed. See, for example, originally filed claims 73 and 77. Claim 79 is believed to be patentable. Indeed, claim 77 is of similar scope and was not rejected by the Examiner in view of Peterson et al.

Claims 80 and 81 each depend from claim 79. Claim 80 recites that the thermal conductivity of the stratum is significantly lower than that of the surface. Claim 81 recites that the thermal conductivity of the stratum is about 1 W/m/K or less. Support for claims 80 and 81 appears in the specification as originally filed. See, for example, page 26, lines 24-27 of the specification.

No new matter has been introduced. Applicants respectfully request reconsideration and allowance of pending claims 23-32 and 73-81 in view of the above amendments and the reasons discussed below.

In addition, applicants request that the Examiner consider the references cited in the supplemental information disclosure (IDS) statement filed on August 13, 2002. A copy of the Form 1449 that accompanied the IDS of August 13, 2002, is enclosed, without references. Applicants request that an initialed copy of the Form 1449 be returned to applicants with the next communication from the Patent Office.

Claim Rejections – 35 USC 112

The Examiner rejected claims 23-32 and 73-77 under 35 USC 112, second paragraph, as being indefinite. Applicants address each of the Examiner's indefiniteness contentions in turn below.

First, the Examiner rejected claim 23 as being incomplete for omitting essential steps. Applicants have amended claim 23 to recite that the connecting of a power source is performed

"to cause current flow through the wafer and a continuous temperature gradient to be formed on a surface of the wafer." No new matter is introduced by this amendment; support for the amendment appears in the specification as originally filed, for example, at page 16, line 9 though page 17, line 12. Applicants submit that claim 23, as amended, is sufficiently definite.

Next, the Examiner rejected claim 24 because it is allegedly unclear what is intended. Specifically, the Examiner stated: "If the temperature sensor in claim 24 is the electrical connector, claim 24 will only have one electrical connector instead of two electrical connectors as recited in claim 23." Applicants respectfully submit that they do not understand the Examiner's point. Claim 24 recites that the temperature sensor is "attached at the same edge of the wafer as the electrical connectors," and that the temperature sensor is also "electrically connected to a temperature controller." Applicants submit that the claim is sufficiently clear.

Finally, the Examiner contended that the term "'low thermal conductivity' in claims 31 and 73 is a relative term," which allegedly renders the claim indefinite. Applicants have amended claims 31 and 73 to recite that the thermal conductivity of the stratum is "significantly lower than that of the surface." No new matter is introduced by this amendment; support for the amendment appears in the specification as originally filed, for example, at page 26, lines 24-27, which discloses that glass, which is one example material for the claimed stratum, has a thermal conductivity between about 0.1-1.0 watts/meter/°K (W/m/K). By contrast, the thermal conductivity of silicon, which is one example material for the claimed surface on which the stratum may be placed, is known to be approximately 160 W/m/K. Applicants submit that claims 31 and 73, as amended, are each sufficiently definite.

Accordingly, applicants submit that rejected claims 23-32 and 73-77 meet the requirements of 35 USC 112, second paragraph, and request that the Examiner withdraw the rejections.

Claim Rejections – 35 USC 102 – Kajiyama et al.

The Examiner rejected claims 23-25 and 29-33 [sic: 29-32] under 35 USC 102(e) as being anticipated by Kajiyama et al. (US Patent No. 6,428,749), filed March 16, 2000.

Specifically regarding independent claim 23 (and dependent claim 29), the Examiner contended:

> [A]s shown in Figures 8, 10, and 18, DNA chip 101 that comprised probe cells on a silicon wafer (semiconducting wafer) as recited in claim 29 was connected to a temperature detection terminal (+) 1003 and a temperature detection terminal (-) 1004, which were connected to the controller comprising a power source. Here two temperature detection terminals were considered as two connectors that were adjacent to each other as recited in claim 23 (see columns 9, 10, 13-15). A temperature gradient could be generated in the DNA chip (see Figure 3 and lines 42-54 in column 11).

The Examiner made further remarks regarding Kajiyama et al. that are relevant to dependent claim limitations.

Applicants respectfully traverse the rejections based on Kajiyama et al., and submit that independent claim 23, as amended, defines an invention that is patentable in view of Kajiyama et al., as do the rejected dependent claims 24-25 and 29-32. Applicants' traversal of the rejections based on Kajiyama et al. should not be taken as a concession by applicants that Kajiyama et al. is properly considered prior art under 35 U.S.C. § 102(e).

The invention, as set forth in independent claim 23, is a method of generating a temperature gradient. The method includes attaching two electrical connectors to a semiconducting wafer. The connectors are adjacent to each other. Each of the connectors is also attached to the wafer at an attachment site. A gap is disposed between the connector attachment sites. The method also includes connecting a power source to the wafer through the two electrical connectors to cause current flow through the wafer and a continuous temperature gradient to be formed on a surface of the wafer.

Kajiyama et al. discloses a biochemical reaction detection chip capable of controlling the temperature for biological reactions including hybridizations. (Abstract; see also col. 2, lns. 30-34.) Figure 1 shows an embodiment of the chip carrying 100 probe cells, each cell being labeled 2. Under each probe cell 2 is an island 4. (See Figure 1C; col. 9, ln. 28). The island 4 is also shown in Figure 2B where it is labeled 21, and is shown in Figure 9. Each probe cell 2 has a heater circuit 5 of an n-type diffuse layer with positive and negative terminals 1001 and 1002 at the ends of the layer 5. (Col. 9, lns. 29-35.) When a voltage is applied across terminals 1001 and 1002, current flows through the n-type diffuse layer 5 to produce Joule heat. (Col. 9, lns. 35-

37.) The amount of heat is controlled by controlling the level or duration of applied voltage. (Col. 9, lns. 37-39.) As shown in Figures 7-9, the n-diffuse layer 77 through which current flows to produce Joule heat is formed in a p-well 73, which in turn is formed on an n-type surface 71. (See col. 12, ln. 51 – col. 14, ln. 22.)

Kajiyama et al. further discloses that the islands 4 are formed in a thermally insulating membrane, and that the islands are spaced apart from each other to also thermally isolate them from one another. (Col. 2, lns. 43-44.) Additionally in some embodiments, such as those shown in Figures 4 and 5, the islands are surrounded by a mesh structure for further thermal isolation of each of the individual islands. (Col. 13, lns. 4-7; see also col. 3, ln. 59 – col. 4, ln. 9.) Thermally isolating the islands 4 from one another is done so that the temperature of each island 4 can be independently controlled. (Col. 3, lns. 26-29; col. 15, lns. 29-30.) Figures 3 and 13, for example, show each island 4 and associated probe cell 2 having a different temperature. In addition, Kajiyama et al. discloses that the temperature of the DNA chip may be computer controlled. (Col. 15, lns. 42-47.)

In Kajiyama et al., each probe cell 2 also has a pn junction 6 and a temperature detection circuit 182 to measure the temperature of the probe cell 2; this is possible because the current-voltage characteristics of the pn junction 6 are largely dependent on the temperature of the pn junction 6. (Figs. 1C & 18; see also col. 9, lns. 36-57.) A controller 105, shown in Figure 18, houses the temperature detection circuit 182, which comprises a power source Vc, resistor R, and voltmeter 110. (Col. 10, lns. 11-13.) The pn junction 6 has a positive (+) temperature detection terminal 1003 and a negative (-) temperature detection terminal 1004. (Col. 9, lns. 36-40.) The temperature detection circuit 182 has a lead connected to terminal 1003 and another lead connected to terminal 1004, as shown in Figure 18.

Kajiyama et al. does not disclose or suggest applicants' invention as set forth in independent claim 23. In particular, Kajiyama et al. does not disclose or suggest attaching a power source to connectors on a semiconducting wafer so that a continuous temperature gradient is formed on a surface of the wafer, as required by independent claim 23.

The Examiner's reference to the Kajiyama et al. power source Vc (Figure 18) shown connected to the two temperature detection terminals 1003 and 1004 cannot support a rejection of independent claim 23, as amended. Indeed, the Kajiyama et al. power source Vc does not

cause current to flow through a semiconductor wafer, but instead causes current to flow through p+ and n+ diffuse layers of the pn junction 6. Moreover, the power source Vc of Kajiyama et al. is not used to cause the formation of a temperature gradient, but instead is used to detect temperature.

Further, the Examiner's reference to Figure 3 and lines 42-54 of column 11 of Kajiyama et al. as allegedly showing the generation of a temperature gradient also cannot support a rejection of claim 23. Figure 3 and the referenced text disclose a structure where each probe cell has a set temperature. Kajiyama et al. discloses a chip 1 that has many conductive silicon islands 4 (also labeled 21 in some figures) each formed on an insulating membrane 22 (see, e.g., column 2, lines 46-42). Each silicon island (4 or 21) has a separate heater circuit consisting of an n-type diffuse layer 5 in which current flows to produce Joule heat. Thermally isolating the islands (4 or 21) from one another is done so that the temperature of each island (4 or 21) can be independently controlled. (Col. 3, lns. 26-29; col. 15, lns. 29-30.) As such, this contrasts with applicants' invention as set forth in independent claim 23 which requires that current flow through a wafer and cause the formation of a continuous temperature gradient on the wafer's surface.

Kajiyama et al. also does not render applicants' invention as set forth in independent claim 23 obvious. Applicants' claimed invention provides testing areas with different temperatures without needing the elaborate and complicated control to achieve each temperature required with the Kajiyama et al. apparatus. Indeed, in this respect, Kajiyama et al. teaches away from applicant's invention.

Accordingly, claim 23 defines an invention that is patentable over Kajiyama et al., as do claims 24-25 and 29-32 which each depend directly or indirectly from claim 23.

Claim Rejections – 35 USC 102 – Peterson et al.

The Examiner rejected claims 73, 74 and 76 under 35 USC 102(b) as being anticipated by Peterson et al. (Journal of Heat Transfer 115, 751-756, 1993). Specifically regarding independent claim 73 (and dependent claim 74), the Examiner contended:

> [A]s shown in Figures 2 and 5, micro heat pump array was fabricated as an integral part of a silicon (two kinds: the rectangular and triangular arrays). At an

input power of 4.0 W, the micro heat array were 68°C and 59.2°C for rectangular and triangular arrays (heat part of a surface) and a copper heat sink temperature was 15 rectangular and triangular arrays (cool part of a surface). The temperature difference between the micro heat pipe array and the sink created a temperature gradient (see page 754). A working buffer flowed from the micro heat pipe array to the sink was considered as a stratum having low thermal conductivity (see page 753).

The Examiner made further remarks regarding Peterson et al. that are relevant to dependent claim 76, which need not be mentioned here.

Applicants respectfully traverse the rejections based on Peterson et al., and submit that independent claim 73, as amended, defines an invention that is patentable in view of Peterson et al., as do the rejected dependent claims 74-77.

Applicants' invention, as set forth in amended independent claim 73, is directed to a method of generating a temperature gradient on a stratum. The method comprises placing the stratum in thermal contact on a surface having a temperature gradient. The stratum has a thermal conductivity that is significantly lower than that of the surface.

Peterson et al. discloses arrays of micro heat pipes integrally fabricated in silicon wafers, or semiconductor devices. (See Abstract.) The heat pipes being fabricated in the semiconductor devices served to increase the effective thermal conductivity of the devices, decrease the temperature gradients occurring across the wafer, decrease the maximum wafer temperatures, and reduce the number and intensity of localized hot spots. (See Abstract.)

Peterson et al. does not disclose applicants' invention as set forth in independent claim 73. In particular, Peterson et al. does not disclose placing a stratum in thermal contact on a surface having a temperature gradient, as is required by claim 73. The Examiner apparently has considered that a "working buffer flow[ing] from the micro heat pipe array and the heat sink" was considered to be the claimed stratum, and refers to page 753 of the reference as support. It is unclear to applicants what it is the Examiner considers to be the claimed stratum. Applicants do not find any reference to a working buffer on page 753, nor can applicants find any mention in the reference of something that flows between the micro heat pipe array and the heat sink. As

such, applicants continue to maintain that their claimed method is novel, and the Examiner has provided no support for his position to the contrary.

In addition, it cannot be said that applicants' invention as set forth in claim 73 is obvious in view of Peterson et al. There is no suggestion in Peterson et al. of a method for generating a temperature gradient on a stratum. Quite differently, Peterson et al. discloses a structure – heat pipes for semiconductor devices – whose purpose it is to reduce the temperature of dense, small-scale semiconductor devices and also reduce the magnitude of temperature gradients generated across such devices.

Accordingly, claim 73 defines an invention that is patentable over Peterson et al., as do claims 74-78 which each depend from claim 73.

CONCLUSION

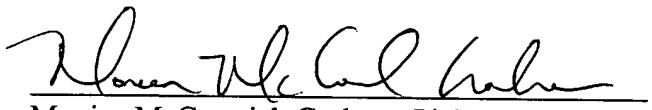
Applicants ask for reconsideration and allowance of pending claims 23-32 and 73-81. The Examiner is invited to telephone the undersigned agent if it is felt that such would advance prosecution of the application.

Attached is a marked-up version of the changes being made by the current amendment.

Enclosed is a $465 check for the Petition for Extension of Time fee. No fee is believed to be due for the added claims. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/3/03



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Version with markings to show changes made

In the claims:

Claims 23, 31, and 73 have been amended as follows:

23. (Amended) A method of generating a temperature gradient comprising:

attaching two electrical connectors to a semiconducting wafer, wherein each of the connectors are adjacent to each other and attached to the wafer at an attachment site with a gap disposed between the attachment sites; and

connecting a power source to the wafer through the two electric connectors to cause current flow through the wafer and a continuous temperature gradient to be formed on a surface of the wafer.

31. (Amended) The method of claim 30 wherein the stratum [comprise low thermal conductivity materials] comprises a material having a thermal conductivity that is significantly lower than that of the surface of the wafer.

73. (Amended) A method of generating a temperature gradient on a stratum comprising placing the stratum in thermal contact on a surface having a temperature gradient, the stratum having [low thermal conductivity] a thermal conductivity that is significantly lower than that of the surface.